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STAGGERED AGC WITH DIGITALLY CONTROLLED VGA

Cross-Reference to Related Applications

BACKGROUND OF THE INVENTION

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Field of Invention

[0001] The invention relates to the field of wireless communications, more particularly to a method of and device for digitally controlled variable gain amplification.

Description of the Related Prior Art

[0002] Rapid growth in the portable communications market has pushed designers to seek low-cost, low-power, highly integrated solutions for the RF transceiver in accordance with the IEEE 802.11a-1999 Part 11: "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications – High Speed Physical Layer in the 5GHz Band which is incorporated herein by reference. As those skilled in the art will appreciate, an automatic gain control (AGC) circuit is a circuit by which gain is automatically adjusted in a specific manner as a function of a specified parameter, such as received signal strength. Gain is the ratio of output current, voltage or power to input voltage or power respectively and is usually expressed in decibels (dB). If the value is less than unity, the dB gain is negative indicating a loss between input and output.

[0003] Radio receivers typically have an AGC algorithm connected to some sort of Variable Gain Amplifier (VGA) which adjusts the gain to compensate for the wide dynamic range of the input signal level. In integrated radio circuits, the use of baseband

VGA's is becoming popular, however, for complex modulation schemes separate in-phase (I) and quadrature (Q) output paths are necessary. As will be appreciated by those in the art, certain radio frequency (RF) applications perform signal processing operations by separating radio frequency signals into signal components representing in-phase and quadrature channels (I and Q channels). For example, in direct conversion receivers, in-phase and quadrature phase signals are utilized to help in demodulating received signals. Generally, signals on the I and Q channel have equal amplitudes and a ninety degree phase difference, and these signals are separately processed by similar circuitry that maintain the amplitude and phase relationships. However, imperfections and mismatches in implementing circuitry may lead to an amplitude or phase imbalance, i.e., a deviation from the ideal amplitude and phase relationships.

[0004] When phase or gain imbalance distorts the received signal, subsequent signal processing is impacted. It is necessary to match the gain and phase of the VGA's used in the baseband AGC. Past solutions have used staggered AGCs with one single analogue control signal for adjusting the gain in an analogue fashion. Alternately, a single stage AGC has been used with a large dynamic range requirement. Neither of the aforementioned solutions has adequately overcome the problem highlighted above.

SUMMARY OF THE INVENTION

[0005] The present invention serves to overcome the deficiencies of the prior art by providing staggered AGCs each associated with respective I and Q digitally controlled VGAs to improve the balance between I/Q paths. Further, the control of the AGCs is done locally to the AGCs rather than globally from a DSP function in the digital portion of the receiver.

[0006] In accordance with a first aspect of the invention there is provided in a wireless receiver wherein a radio frequency signal is received, downconverted and processed into in-phase (I) and quadrature (Q) signal paths, a method of automatic gain control (AGC) comprising the steps of: (a) at a specified stage in an I/Q baseband strip

containing multiple automatic gain control (AGC) stages: (i) detecting respective I and Q output signals received from respective I and Q variable gain amplifiers (VGAs) associated with the specified AGC stage; (ii) digitizing the detected I and Q signals; (iii) adjusting the respective I and Q variable gain amplifiers (VGAs) for differences between the detected I and Q output signals and a reference signal; and (b) repeating step (a) through each AGC stage.

[0007] In accordance with a second aspect of the invention there is provided in a wireless receiver wherein a radio frequency signal is received, downconverted and processed into in-phase (I) and quadrature (Q) signal paths, an automatic gain control (AGC) circuit comprising an I/Q baseband strip comprising multiple AGC stages wherein each of the AGC stages comprises: respective I and Q variable gain amplifiers (VGAs); a detector for detecting respective I and Q output signals received from the respective I and Q variable gain amplifiers (VGAs); an analogue to digital converter (ADC) for converting the detected I and Q output signals; and a digital engine for digitally adjusting the respective I and Q variable gain amplifiers (VGAs) for differences between the detected I and Q output signals and a reference signal.

[0008] The advantages of the present invention are now readily apparent. The use of staggered AGCs incorporating respective I and Q VGAs means that the total dynamic range is split between n-stages. This means that respective I and Q VGAs have reduced gain requirements and are easier to design. In addition, the use of digital control for setting the VGA gains means that analog variations are reduced and the I/Q gain imbalances can be reduced compared to using analog controlled VGA's. Finally, using locally generated feedback (as opposed to globally generated feedback) allows for the optimum arrangement for interleaved VGA's since there is typically a transport (group) delay of the signals through the interleaved blocks. By staggering the control of the VGAs in time as opposed to one single control (as in global feedback systems), improved dynamic settling can be obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] A better understanding of the invention will be obtained by considering the detailed description below, with reference to the following drawings in which:

Figure 1 depicts a block diagram of a digital receiver in accordance with the present invention;
Figure 2 depicts a block diagram of a digital demodulator integral to the digital receiver of Figure 1;
Figure 3 depicts an I/Q baseband strip of the digital demodulator front-end of Figure 2;
Figure 4 depicts a more detailed view of the I/Q baseband strip of Figure 3;
Figure 5 depicts the digitally controlled variable gain amplifier (VGA) architecture in accordance with the present invention;
Figure 6 depicts in greater detail the detector within the architecture of Figure 5;
Figure 7 depicts an analogue-to-digital (ADC) converter used in association with a two level detector;
Figure 8 depicts an analogue-to-digital (ADC) converter used in association with a four level detector;
Figure 9 depicts in greater detail the digital engine within the architecture of Figure 6;
Figure 10 depicts a graph representing the counter action versus time of the up/down counter of Figure 9; and
Figure 11 depicts a graph similar to the graph of Figure 10, but which includes four target zones.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[00010] Referring to Figure 1, there is depicted a digital receiver 10 in which the present invention is housed. The preferred receiver may be, for example, the ICE5350 Digital Receiver offered by IceFyre Semiconductor Inc. which performs all the physical layer functions detailed in the IEEE 802.11a standard, but the invention is not meant to be limited to this receiver. The digital receiver is located between the RF Receiver Front

End 12 and the Physical Medium Access Control (PHY/MAC) 14. The RF Receiver Front End connects to antennae A and B. As shown in the drawing, the two main blocks within the digital receiver 10 are the digital demodulator 16 and the baseband decoder 18. The digital demodulator 16 recovers the baseband signal by removing carrier offsets, timing offsets, compensating for the channel impairments and demapping the digitally modulated signal. This block is located between the analog-to-digital interface (not shown) and the baseband interface (not shown). The baseband decoder 18 de-interleaves the baseband signal, provides error correction through the soft-decision Viterbi algorithm and unscrambles the corrected bit stream to be passed through the PHY/MAC 14. This block is located between the baseband interface (not shown) and the PHY/MAC interface (not shown).

[00011] Figure 2 depicts the digital demodulator 16 of Figure 1. As shown in the diagram, the analog to digital interface is located at block ADCs/ DACs 20. The baseband interface can also be seen in the figure at the soft decision demapper 22. It can also be seen in the figure that the digital demodulator 16 is distinctly divided into two parts by the Fast Fourier Transform (FFT) circuit 24. To the left is the digital demodulator front-end (DFE) 26, while to the right is the digital demodulator back-end (DBE) 28. The invention of the present invention is provided in the digital demodulator front-end 26.

[00012] More specifically, the invention is contained in the baseband I/Q strip containing multiple AGC stages, as more clearly depicted in Figure 3. As shown in the figure, received radio frequency (RF) signals are processed by a low noise amplifier (LNA) mixer downconverter 30. A local oscillator signal is mixed with a high frequency (e.g. 400 – 2500Mhz) RF input signal which is then downconverted to a lower intermediate frequency (IF) (e.g. 10MHz to 500MHz) output signal. As will be appreciated, a quadrature generator (not shown) functions as a signal source that provides in-phase (I) and quadrature (Q) signals to the I/Q baseband strip 32. The LNA mixer 30 combines the I and Q signals with the RF signals, thereby separating the RF signals into I and Q components to facilitate demodulation. The I and Q components are

fed to the I/Q baseband strip 32. As will also be appreciated, the I/Q baseband strip is analogous to an IF strip in a radio receiver which allows certain analogue functions such as amplification and filtering to be performed at a lower frequency than the received frequency.

[00013] Referring to Figure 4, a more detailed description of the I/Q baseband strip 32 of Figure 3 is provided. As can be seen from the drawing, generally speaking I/Q baseband strip 32 is divided into a series of AGC stages, two of which are shown at 34 and 36. AGC circuits 38, 40 containing VGAs 42 are distributed between low pass filters (LPFs) or buffer amplifiers 44, and receive feedback from LPFs or buffer amplifiers 44 immediately after these components. As those skilled in the art will appreciate, an LPF is a filter that passes all frequencies below a specified frequency with little or no loss but strongly attenuates high frequencies. Depending on the application, the AGC feedback control signal may come before or after LPFs or buffer amplifiers 44.

[00014] Figure 5 depicts a single AGC stage of I/Q baseband strip 32 of Figure 4, describing in greater detail the digitally controlled VGA architecture of the present invention. An I/Q detector 46 detects the power in I/Q signal paths (shown as I output and Q output) extending from respective VGAs 42. The architecture also includes an analogue to digital converter (ADC) 48 to digitize the detected I/Q output signals and a digital engine 50 to process differences between the detected I/Q output signals and a reference, as will be more fully described in relation to Figure 9.

[00015] Referring to Figure 6, the detector of Figure 5 is described in more detail. I/Q output signals are fed to respective high pass filters (HPF) which are used to remove direct current (DC) offsets which would bias the input of detector 46. The I/Q signals then flow to respective rectifiers 54 which change the alternating current I/Q output signals to direct current, and subsequently to an operation amplifier (op-amp) 56 which adds the I/Q signals together. The resulting signal is then sent to a low pass filter (LPF) 58.

[00016] Figures 7 and 8 highlight alternate analogue to digital converters (ADCs) 48 for the system of Figure 5. The ADCs use a simple multi-level comparator 60 and some logic 62 to generate the up/down and count/hold control signals for the counter 64. The ADC 48 function can be increased to four or more levels. As will be understood by those in the art, a comparator is used to compare two numbers, to determine if a given signal is bigger or smaller than some reference voltage. This can be accomplished using a simple circuit, such as an op-amp that has no feedback. If a difference or error beyond a predefined range or boundary is determined, the gain of VGAs 42 is adjusted accordingly.

[00017] Figure 9 depicts the digital engine 50 of the system of Figure 5. The up/down and count/hold control signals generated by ADC 48 (Figure 5) are fed to up/down counter 64. As described above, if the difference between the detected I/Q output signals and a reference (shown as Vref/force in Figure 9) is sufficiently large, the gains of the digitally controlled VGAs 42 are adjusted by the counter 64 to bring the I/Q output signals to within a "target zone", as discussed in relation to Figure 10. More specifically, the gain will either be held at its present/desired value, or adjusted up or down until the desired level is met.

[00018] Figures 10 depicts a graph representing the counter action versus time of the up/down counter of Figure 9. As shown in the figure, the counter tries to achieve a "target zone" extending between Vth_Upper and Vth_Lower. When Vnom is reached, the gain is held. As shown in Figure 11, this concept can be extended to more than one level e.g. four target zones are depicted. As shown in the Figure, the gain will be adjusted at a fast rate with a fixed amplitude increment if the detected error is well outside the defined range, and at a slower rate with a fixed amplitude increment as the target zone is approached. This dual-speed option improves dynamic settling of the AGC system. Alternately, it is possible to adjust the gain control at a fixed rate, but with a large amplitude increment if the detected error is well outside the defined range and with a small amplitude increment as the target zone is approached.

[00019] In essence, staggered AGCs are arranged by employing digitally controlled VGAs and a closed feedback loop control system for respective I and Q VGAs within each AGC stage. The output signals from respective I and Q VGAs is detected to determine if adjustment to the VGA gain is required. The detected I/Q output signal is digitized and converted to digital control signals which are ultimately fed to the respective I and Q VGAs. For a received RF signal, this process is completed by each AGC stage within the staggered AGC architecture, with the goal of providing a consistent output signal from the digital demodulator front-end.

[00020] As will be understood by those skilled in the art, the present invention relates to integrated circuits in which a staggered AGC incorporating digitally controlled VGAs is used in combination with other components to form a useful circuit within an integrated circuit. The individual electronic and processing functions utilized in the foregoing described embodiment are, individually, well understood by those skilled in the art. It is to be understood by the reader that a variety of other implementations may be devised by skilled persons for substitution and the claimed invention herein is intended to encompass all such alternative implementations, substitutions and equivalents. Persons skilled in the field of electronic and integrated circuit design will be readily able to apply the present invention to an appropriate implementation for a given application.

[00021] Consequently, it is to be understood that the particular embodiments shown and described herein by way of illustration are not intended to limit the scope of the invention claimed by the inventors/assignee, which is defined by the appended claims.